IN THE CLAIMS

1. (original) An RF power amplifier formed using an integrated circuit, comprising:

a power amplifier circuit; and

a serial interface formed using the integrated circuit for sending and receiving signals.

2. (original) The RF power amplifier of claim 1, wherein the integrated circuit includes a plurality of pins, the RF power amplifier further comprising:

a mode control pin for selecting a first mode or a second mode; and

a first interface pin, wherein the first interface pin has a first function in the first mode and a second function in the second mode.

3. (original) The RF power amplifier of claim 2, further comprising a second interface pin, wherein the second interface pin has a first function in the first mode and a second function in the second mode.

4. (original) The RF power amplifier of claim 2, wherein the first mode is a serial interface mode and the second mode is a pin control mode.

5. (original) The RF power amplifier of claim 2, wherein the mode control pin is used as an internal voltage source in the power amplifier.

6. (original) The RF power amplifier of claim 5, wherein the mode control pin is used as an internal voltage source in the power amplifier only when the first mode is selected.

7. (original) The RF power amplifier of claim 1, wherein the RF power amplifier further comprises:

a plurality of pins for coupling to a serial bus; and

a low pass filter coupled to one of the pins for filtering control signals to reduce RF noise.

8. (original) The RF power amplifier of claim 1, wherein the RF power amplifier further comprises:

a plurality of pins for coupling to a serial bus; and

a gate circuit coupled to a first pin for selectively blocking the signal received at the first pin.

9. (original) The RF power amplifier of claim 8, wherein the signal is blocked when the RF power amplifier is enabled.

10. (original) The RF power amplifier of claim 8, wherein the first pin receives a serial clock signal.

11. (original) The RF power amplifier of claim 1, wherein the RF power amplifier further comprises:

a serial data output pin for coupling to a serial bus; and

a tri-state driver coupled to the serial data output pin.

12. (original) The RF power amplifier of claim 11, wherein the tri-state driver tri-states the output pin while the RF power amplifier is transmitting.

13. (original) The RF power amplifier of claim 12, further comprising a bias circuit for biasing the tri-stated output pin while the RF power amplifier is transmitting.

14. (original) A wireless communication device comprising:

a controller circuit adapted to control the operation of the communication device;

a transceiver;

an RF power amplifier; and

a serial bus coupled to the controller, transceiver, and RF power amplifier.

15. (original) The wireless communication device of claim 14, wherein the power amplifier includes a sensor for sensing a property of the power amplifier.

16. (original) The wireless communication device of claim 15, wherein information from the sensor is transmitted to the controller over the serial bus.

17. (original) The wireless communication device of claim 16, wherein the sensor is a temperature sensor.

18. (original) The wireless communication device of claim 14, wherein the controller transmits a band control signal to the transceiver over the serial bus, and wherein the power amplifier monitors the serial bus and automatically selects a band based on the band control signal.

19. (original) The wireless communication device of claim 14, wherein the serial bus is disabled when the power amplifier is enabled.

20. (original) The wireless communication device of claim 14, wherein the power amplifier includes a mode control pin which selects a serial interface mode or a pin control mode.

21. (original) The wireless communication device of claim 20, further comprising a coupling between the controller and the mode control pin, wherein the controller supplies the power amplifier with a voltage supply via the connection to the mode control pin.

22. (original) The wireless communication device of claim 14, wherein the serial bus is disabled when the power amplifier is transmitting.

23. (original) The wireless communication device of claim 14, wherein the power amplifier further comprises:

a plurality of pins for coupling to a serial bus; and

a low pass filter coupled to one of the pins for filtering control signals to reduce RF noise.

24. (original) The wireless communication device of claim 14, wherein the power amplifier further comprises:

a plurality of pins for coupling to a serial bus; and

a gate circuit coupled to a first pin for selectively blocking the signal received at the pin.

25. (original) The wireless communication device of claim 24, wherein the signal is blocked when the power amplifier is enabled.

26. (original) The wireless communication device of claim 25, wherein the first pin receives a serial clock signal.

27. (original) The wireless communication device of claim 14, wherein the power amplifier further comprises:

a serial data output pin for coupling to a serial bus; and

a tri-state driver coupled to the serial data output pin.

28. (original) The wireless communication device of claim 27, wherein the tri-state driver tri-states the output pin while the power amplifier is transmitting.

29. (original) The wireless communication device of claim 28, further comprising a bias circuit for biasing the tri-stated output pin while the power amplifier is transmitting.

30. (original) A method of controlling an RF power amplifier in a wireless communications device, comprising:

providing a baseband controller connected to a digital bus;

providing an RF power amplifier having a serial interface for communicating with the digital bus; and

coupling the serial interface of the RF power amplifier to the digital bus.

31. (original) The method of claim 30, wherein the power amplifier transmits signals in periodic bursts, and wherein the digital bus is disabled during the bursts.

32. (original) The method of claim 30, wherein the serial interface of the power amplifier uses a plurality of pins, the method further comprising the step of coupling a low pass filter to at least one of the pins.

33. (original) The method of claim 30, wherein the serial interface of the power amplifier uses a plurality of pins, the method further comprising the step of blocking the signal provided to a first pin of the power amplifier serial interface when the power amplifier is transmitting.

34. (original) The method of claim 30, further comprising providing a serial data output pin at the serial interface of the power amplifier; and when the power amplifier is transmitting, biasing the serial data output pin.

35. (original) The method of claim 30, further comprising providing a serial data output pin at the serial interface of the power amplifier; and when the power amplifier is transmitting, tri-stating the serial data output pin.

36. (original) The method of claim 35, further comprising biasing the tri-stated output pin.

37. (original) The method of claim 30, further comprising sensing a condition in the power amplifier; and sending information relating to the sensed condition over the digital bus.

38. (original) The method of claim 37, wherein the sensed condition is temperature.

39. (original) The method of claim 37, further comprising shutting down the RF power amplifier in response to the sensed condition.

40. (original) The method of claim 39, the RF power amplifier is shut down when a threshold temperature is sensed.

41. (new) The method of claim 30, wherein the RF power amplifier includes a plurality of pins, the method further comprising selecting between first and second modes of operation by applying a control signal to a mode control pin.

42. (new) The method of claim 41, further comprising providing a first interface pin, wherein the first interface pin has a first function in the first mode of operation and a second function in the second mode of operation.

43. (new) The method of caim 42, further comprising providing a second interface pin, wherein the second interface pin has a first function in the first mode of operation and a second function in the second mode of operation.

44. (new) The method of claim 41, wherein the first mode of operation is a serial interface mode and the second mode of operation is a pin control mode.

45. (new) The method of claim 30, wherein the baseband controller transmits a band control signal to the RF power amplifier over the digital bus, and wherein the RF power amplifier monitors the digital bus and automatically selects a band based on the band control signal.